This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS

1-6. (cancelled).

7. (previously presented) A method for system simulation with simulated microcontrollers/microprocessors and appertaining peripheral modules, said method comprising the steps of:

in a first sequence of steps, simulating said microcontroller/microprocessor and said peripheral modules with predetermined signal patterns, said first sequence of steps having markers inserted therein;

in a second sequence of steps, interrogating and evaluating states of said system brought about by said simulation; and

interrupting said first sequence of steps for executing said second sequence of steps as dictated by said markers inserted into said first sequence, said second sequence of steps being executed in an accelerated operational mode that is adapted to said evaluation.

8. (previously presented) The method as claimed in claim 7, wherein said first sequence of steps provides a clock-cycle-based simulation of said microcontroller/microprocessor and of said peripheral modules.

9. (currently amended) The method as claimed in claim 7, wherein said first sequence of steps is a series of consecutive program codes corresponding to program codes of at least one of the modules to be simulated.

10. (previously presented) The method as claimed in claim 9, wherein said markers are formed by one of opcodes or opcode sequences that are not usually used in said program code.

11. (previously presented) The method as claimed in claim 7, wherein peripheral modules that were specified during said second sequence of steps are functionally cosimulated.

12. (cancelled).

13. (new) An apparatus for carrying system simulation, comprising:

a simulated microcontroller or microprocessor module that simulates a component to be tested with the system simulation;

a simulated peripheral module that simulates a component to be tested with the system simulation;

a first sequence of steps comprising markers that are inserted into the first sequence of steps, the first sequence of steps being configured to simulate at least one of the microprocessor, microcontroller, and peripheral;

system states that are induced by the first sequence of steps;

a second sequence of steps configured to interrogate and evaluate the system states in response to an interrupt of the first sequence of steps triggered by the markers, the second sequence of steps being configured to be executed in an accelerated operational mode that is adapted to the evaluation; and

a microprocessor control unit comprising a signal pattern generator configured for simulating one of the modules by generating signal patterns with an essentially precise clock cycle and configured for

interrogating and evaluating states of one or more of the modules that are brought about by the simulation during a program interrupt by activating an instruction set simulator.

5